PATENT ABSTRACTS OF JAPAN

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(71)Applicant : NEC CORP
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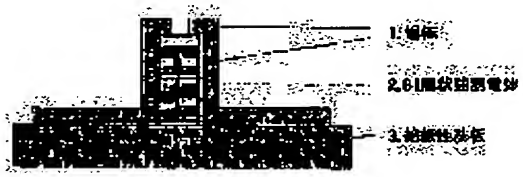
(54) CAPACITOR WHICH USES LAMINAR BISMUTH FERROELECTRIC MATERIAL AND MANUFACTURE OF THIS CAPACITOR

(57)Abstract:
PURPOSE: To increase the density of a capacitor element which uses ferroelectric material and reduce the driving voltage by efficiently use the residual polarization of the laminar bismuth ferroelectric material.
CONSTITUTION: A capacitor which uses laminar bismuth ferroelectric material of c-axis orientation is provided by arranging a pair of electrodes 1 which are composed of a first and second electrodes, and permitting the pair of electrodes 1 to have relative position relation that generates an electric field in a direction parallel to a substrate 3 at a part within the ferroelectric material 2. The pair of electrodes 1 are preferably arranged so as to apply the electric field in the maximum polarization direction or mainly in such direction. After forming the laminar bismuth ferroelectric material 2 of c-axis orientation, the maximum polarization direction of the film is detected, and the capacitor is provided by the manufacture that forms the pair of electrodes 1 which apply electric field mainly in this direction.



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* NOTICES *

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CLAIMS

[Claim(s)]
[Claim 1] The capacitor using the bismuth stratified ferroelectric characterized by preparing the electrode of a pair which consists of the 1st and 2nd electrode which generates the electric field of a direction parallel to a substrate side at least in the part in said ferroelectric in contact with said ferroelectric in the capacitor which has a c-axis orientation bismuth system stratified ferroelectric and an electrode on an insulating substrate.
[Claim 2] The capacitor using the bismuth system stratified ferroelectric according to claim 1 characterized by preparing the electrode of a pair in the location where the greatest electric field are impressed in the direction of the maximum polarization of a c-axis orientation bismuth system stratified ferroelectric.
[Claim 3] The manufacture approach of the capacitor using the bismuth system stratified ferroelectric which forms a c-axis orientation bismuth system stratified ferroelectric on a substrate, and is characterized by consisting of the 1st process which carries out patterning, and the 2nd process which forms one pair of electrodes in said ferroelectric.
[Claim 4] The manufacture approach of the capacitor using the bismuth system stratified ferroelectric according to claim 3 characterized by forming one pair of electrodes which detect the direction of the maximum polarization of said ferroelectric after forming a ferroelectric, or after performing patterning, and may impress electric field in the detected direction of the maximum polarization in the ferroelectric front face by which patterning was carried out.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] It is related with the capacitor using a bismuth system stratified ferroelectric, and its manufacture approach.
[0002]
[Description of the Prior Art] A bismuth system stratified ferroelectric is an ingredient with which the application to nonvolatile memory is expected with the structure where the pseudo-perovskite structure was inserted into the bisumuth-oxide layer. Although the ferroelectricity makes the origin the variation rate of B site ion of the pseudo-perovskite part pinched by the bisumuth-oxide layer, its anisotropy over a crystallographic axis is strong, and it is understood that the ferroelectricity of the direction of an a-axis is large compared with the ferroelectricity of the direction of a c-axis.
[0003] As capacitor structure using such [conventionally] an ingredient, it is an international patent, for example. WO There is a thing as shown also in 93/12542 (International Patent Publication Number WO 93/12542). The basic structure was the structure which carried out the laminating of the ferroelectric thin film 2 on both sides of the up electrode 5 and the lower electrode 6 on the insulating substrate 3 as shown in drawing 7 .
[0004]
[Problem(s) to be Solved by the Invention] A bismuth stratified ferroelectric has an anisotropy over a crystallographic axis in a remanence, and it is the direction of an a-axis that the maximum remanence is acquired, and it turns out that the remanence of the direction of a c-axis is very small. however, the case where this ingredient is thin-film-ized -- physical vapor growth (PVD), such as a spatter and vacuum deposition, -- law and chemical vapor growth (CVD) -- it was difficult for the c-axis orientation film to have been easy to be obtained by the conventional growth approaches, such as law, and to have made the orientation of the greatest polarization shaft orientations carry out in the direction perpendicular to a substrate side. For this reason, with the conventional component structure which is the structure of impressing electric field to a substrate side and a perpendicular direction, a remanence could not be used effectively but there was a problem that detailed-izing of a component and low-battery-izing were difficult.
[0005] moreover -- general -- the time of bismuth stratified ferroelectric thin film membrane formation -- the elevated temperature of 700 or more C -- required -- in addition -- and since it was exposed into an oxidizing atmosphere, in the laminated structure of a lower electrode, a ferroelectric, and an up electrode, it was difficult for the defective continuity by oxidation of a lower electrode, and the reaction of a ferroelectric and a lower electrode to get angry at the time of ferroelectric membrane formation, and to produce the component of a good property.
[0006] The purpose of this invention is to offer the structure and the manufacture approach of a capacitor which canceled the above-mentioned conventional fault.
[0007]
[Means for Solving the Problem] This invention is characterized by preparing the electrode of a pair which consists of the 1st and 2nd electrode which generates the electric field of a direction parallel to a substrate side at least in the part in said ferroelectric in the capacitor which has a c-axis orientation bismuth system stratified ferroelectric and an electrode in contact with said ferroelectric on an insulating substrate. At this time, since an electrode can achieve much more low-battery-ization by being prepared in the location where the greatest

electric field are impressed in the direction of the maximum polarization of a c-axis orientation bismuth system stratified ferroelectric, it is desirable.

[0008] Moreover, the manufacture approach of the bismuth system stratified ferroelectric capacitor by this invention is characterized by consisting of the 1st process which forms a c-axis orientation bismuth system stratified ferroelectric on a substrate, and carries out patterning, and the 2nd process which forms one pair of electrodes in said ferroelectric. Here, if the direction of the maximum polarization of said ferroelectric is detected after forming a ferroelectric, or after performing patterning, one pair of electrodes which may impress electric field in the detected direction of the maximum polarization can also be formed in the ferroelectric front face by which patterning was carried out.

[0009]

[Function] The capacitor structure by this invention is shown in drawing 1 . The remanence of the direction of an a-axis restricted in the field parallel to a substrate side can be effectively used using the electrode of a pair by impressing electric field parallel to a substrate side to the c-axis orientation bismuth stratified ferroelectric on an insulating substrate. That is, since a charge required of a small electrode surface product can be obtained, detailed-ization of a component can be attained. Moreover, by producing an electrode after ferroelectric membrane formation, the reaction of the ferroelectric film and electrode under an elevated temperature and oxidation of an electrode are controlled, and improvement in the dependability of a component can be aimed at. Furthermore, since an effective charge consistency becomes high further when having mainly gathered in the one direction in the field where the direction of the maximum part polar axis is parallel to a substrate side, polarization reversal of a capacitor is attained by smaller electric field, and the further low-battery-izing is possible.

[0010]

[Example]

(Example 1) The example at the time of using RF magnetron sputtering as the membrane formation approach of SBT is shown in drawing 2 as a bismuth stratified ferroelectric, using W as a strontium acid tantalic acid bismuth (SrBi2 Ta 2O9, henceforth, SBT), the silicon substrate by which scaling processing was carried out as an insulating substrate, and an electrode material. The capacitor production procedure was as follows. It is 1 micrometer with the RF magnetron sputtering method on the silicon substrate by which scaling processing was carried out. Production of SBT of thickness formed the SBT thin film which carried out orientation to the c-axis at 700 or more C of substrate temperature. Then, it is 0.5 micrometers of bases about this SBT thin film. x5micrometer Height of 1 micrometer It is 0.3 micrometers about W with the CVD method after carrying out etching processing at convex structure. It deposited on thickness. 1 micrometer of after that SBT convex structure x5micrometer It left the side face and the connected drawer electrode, and etching removal of the W was carried out. At this time, it is 1 micrometer. x5micrometer Two drawer electrodes of a field are connected with the drawer electrode from the same side face of other components, and have structure which connected two or more capacitors to juxtaposition. The hysteresis characteristic acquired with the capacitor of this structure is shown in drawing 3 . The property of structure was also shown in coincidence conventionally which sandwiched the ferroelectric with Pt electrode of the upper part and the lower part as a candidate for a comparison. When the laminating of the electrode is carried out up and down (alternate long and short dash line), a remanence value is 1.4microC/cm2. To very small one, when electric field parallel to a substrate are impressed (continuous line), it is C/cm2 10.5micro. It became, the remarkable increment in a remanence value was seen, and it was shown that densification of a component can be attained.

[0011] (Example 2) The case where RF magnetron sputtering is used as the membrane formation approach is shown as a bismuth stratified ferroelectric, using W as a strontium acid niobic acid bismuth (SrBi2Nb 2O9, henceforth, SBN) or a titanic-acid bismuth (Bi4 Ti 3O12, henceforth, BIT), the silicon substrate by which surface treatment was carried out as an insulating substrate, and an electrode material. The capacitor production procedure is the same as that of an example 1. The strong dielectric characteristics obtained with the capacitor of this structure are shown in Table 1. Although the absolute value of a remanence was small, when electric field parallel to a substrate as well as the case where it is the SBT film were impressed, the increment in a remanence value was seen, and it was shown that densification of a component can be attained.

[0012]

[Table 1]

強誘電体	印加電界 (kV/cm)	上下積層型の残留分極値 ($\mu C/cm^2$)	本発明型の残留分極値 ($\mu C/cm^2$)
SBN	300	1.1	5.2
BIT	200	1.9	5.5

[0013] (Example 3) SBT was formed by the same approach as an example 1, using a MgO single crystal (100) side as an insulator substrate, and the same capacitor structure as an example 1 was formed. In this case, since a SBT thin film grew epitaxially to a MgO substrate, the direction of polarization had gathered also in the field parallel to a substrate. In order to determine the direction which impresses electric field, the electrode group of the shape of a dot like drawing 4 was produced on the SBT film front face, and the remanence was measured by 2 terminal method between F from Electrode A and Electrode B, respectively. An example of a measurement result is shown in drawing 5 . In this case, it turned out that the polarization value between Electrode A and Electrode D is the largest, and this direction is the direction of the maximum part polar axis. According to this result, the electrode was formed so that an electrical potential difference might be impressed to the direction of electrode A-D, and parallel. The hysteresis characteristic of polarization acquired with the capacitor of this structure is shown in drawing 6 . The property of the same sample that Pt electrode was formed in the upper part and the lower part as a candidate for a comparison is shown. To a hysteresis characteristic hardly being shown, when the laminating of the electrode is carried out up and down (alternate long and short dash line), when electric field parallel to a substrate are impressed (continuous line), it is 13.7microC/cm2. It became and the remarkable increment in a remanence value was seen. When electric field parallel to the substrate of an example 1 were impressed, even if it compared, it increased 30% with the remanence value, and it was decreasing 22% by the coercive electric field, and it was shown that densification of a component and low-battery-ization can be attained.

[0014] In addition, the ingredient used in the above example is the example of 2 and 3, and this invention is not limited to the ingredient stated in the above example, but is a c-axis orientation ferroelectric, and can be applied to all the ingredients that are not in agreement with a c-axis by the direction of the maximum polarization.

[0015]

[Effect of the Invention] By using the component structure by this invention, effective use of the remanence of a bismuth stratified ferroelectric can be attained, and the densification of a component and reduction of driver voltage are possible as a result. Furthermore the defective continuity of a lower electrode decreases in number, and high reliance-ization can be realized.

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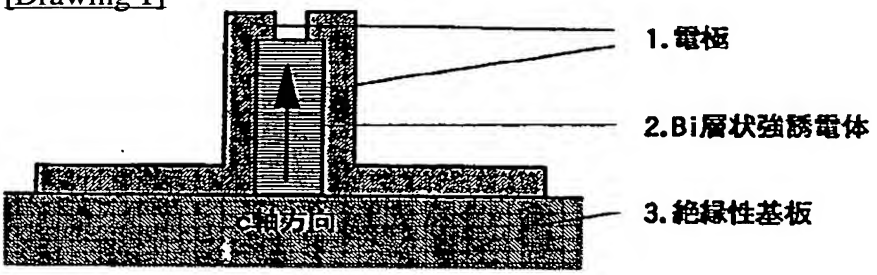
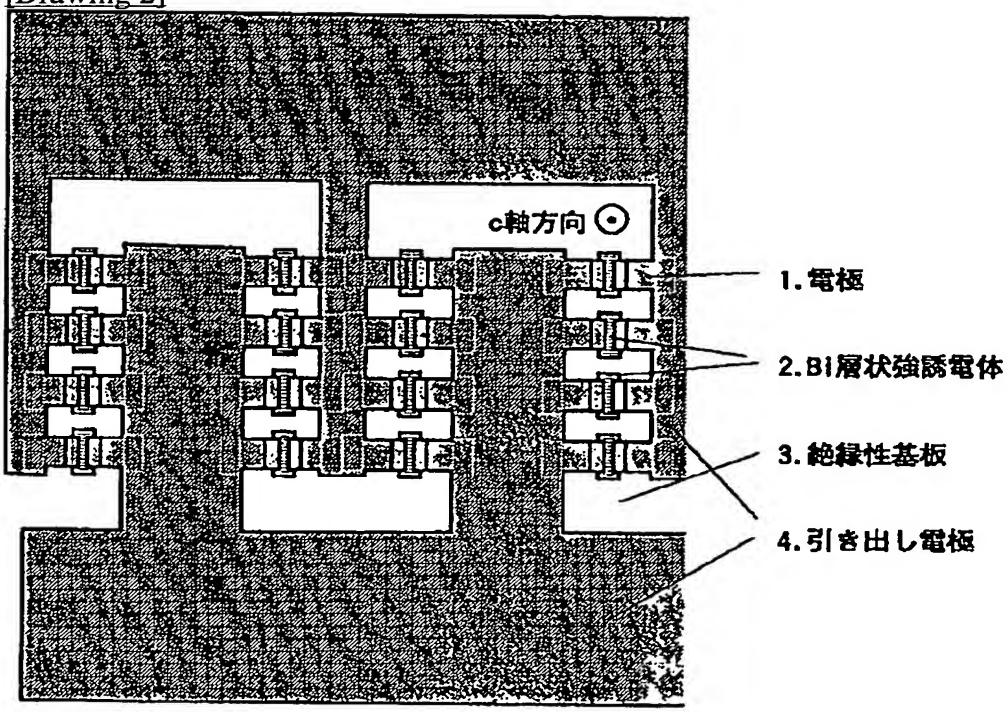
DRAWINGS

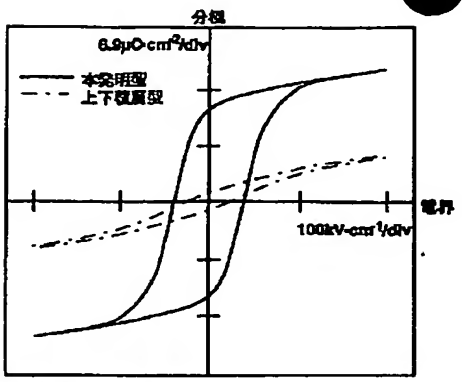
[Drawing 1]



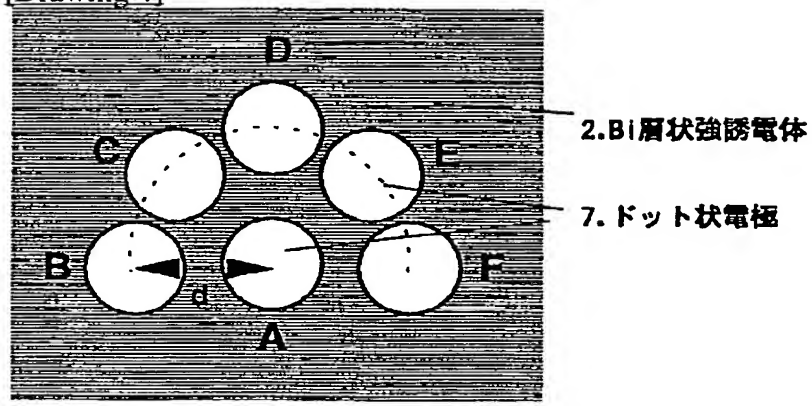
[Drawing 2]



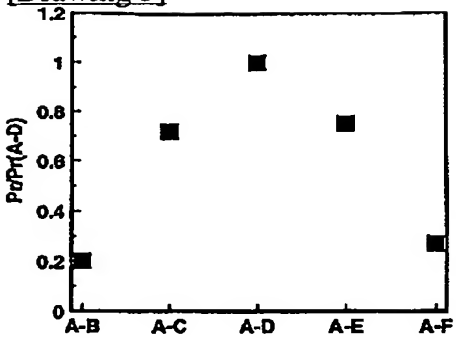
[Drawing 3]



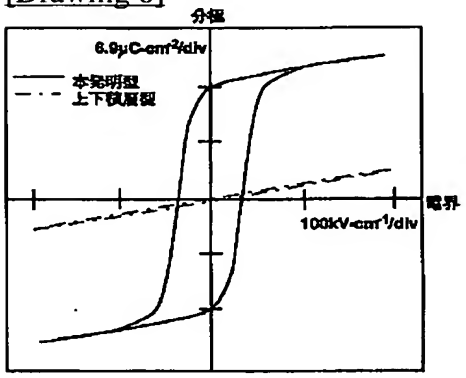
[Drawing 4]



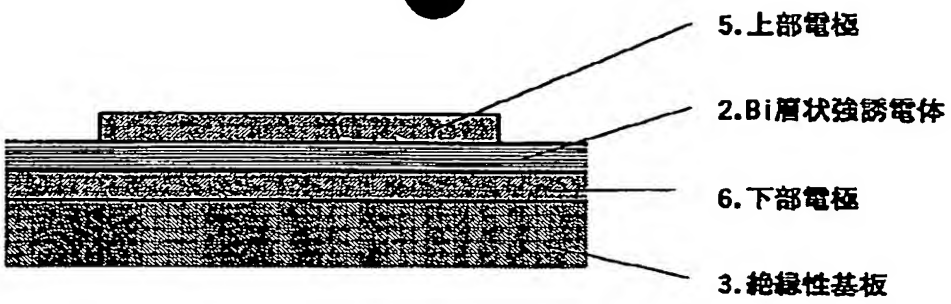
[Drawing 5]



[Drawing 6]



[Drawing 7]



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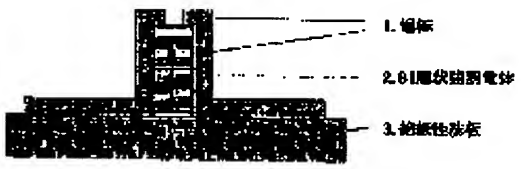

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Ｃ０１Ｇ	33/00				35/00	Ｃ	
	35/00		7202－4G	Ｃ３０Ｂ	29/30	Ａ	
Ｃ３０Ｂ	29/30		7202－4G			Ｂ	

審査請求　有　請求項の数４　ＯＬ　（全　５　頁）　最終頁に続く

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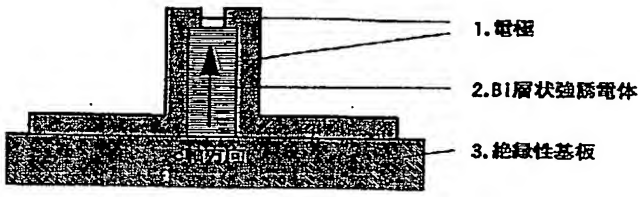
(54)【発明の名称】　ビスマス系層状強誘電体を用いたキャパシタとその製造方法

(57)【要約】

【目的】　ビスマス層状強誘電体の残留分極を有効に利用することにより、この強誘電体を用いたキャパシタ素子の高密度化、駆動電圧の低減をはかる。

【構成】　ｃ軸配向ビスマス系層状強誘電体を用いたキャパシタにおいて、強誘電体２に第１、第２の電極からなる一対の電極１が配置され、その一対の電極１が、強誘電体２中の一部に基板３と平行な方向の電界を発生することが可能な相対的位置関係を有することを特徴とするキャパシタである。ここで、１対の電極１が最大分極方向、又は、主にその方向に電界を印加するように配置されていることが好ましい。このようなキャパシタは、ｃ軸配向ビスマス系層状強誘電体２を形成した後、その膜の最大分極方向を検出し、その後、主にその方向に電界を印加する１対の電極１を形成することを特徴とする製造方法によって得られる。



【特許請求の範囲】
【請求項１】絶縁性基板上にｃ軸配向ビスマス系層状強誘電体及び電極を有するキャパシタにおいて、前記強誘電体中の少なくとも一部分に基板面と平行な方向の電界を発生する第１、第２の電極からなる一対の電極が、前記強誘電体に接して設けられていることを特徴とするビスマス層状強誘電体を用いたキャパシタ。
【請求項２】一対の電極が、ｃ軸配向ビスマス系層状強誘電体の最大分極方向に最大の電界が印加される位置に設けられていることを特徴とする請求項１記載のビスマス系層状強誘電体を用いたキャパシタ。
【請求項３】基板上にｃ軸配向ビスマス系層状強誘電体を形成し、パターニングする第１の工程と、前記強誘電体に１対の電極を形成する第２の工程とからなることを特徴とするビスマス系層状強誘電体を用いたキャパシタの製造方法。
【請求項４】強誘電体を形成した後、もしくはパターニングを行った後に前記強誘電体の最大分極方向を検出し、検出された最大分極方向に電界を印加しうる１対の電極をパターニングされた強誘電体表面に形成することを特徴とする請求項３記載のビスマス系層状強誘電体を用いたキャパシタの製造方法。
【発明の詳細な説明】
【０００１】
【産業上の利用分野】ビスマス系層状強誘電体を用いたキャパシタとその製造方法に関する。
【０００２】
【従来の技術】ビスマス系層状強誘電体は擬ペロブスカイト構造が酸化ビスマス層に挟まれた構造を持ち不揮発メモリへの応用が期待される材料である。その強誘電性は酸化ビスマス層に挟まれた擬ペロブスカイト部分のＢサイトイオンの変位を起源としているが結晶軸に対する異方性が強く、ｃ軸方向の強誘電性に比べａ軸方向の強誘電性が大きいことがわかっている。
【０００３】従来このような材料を用いたキャパシタ構造としては、例えば、インターナショナルパテント　ＷＯ　９３／１２５４２（Ｉｎｔｅｒｎａｔｉｏｎａｌ　Ｐａｔｅｎｔ　Ｐｕｂｌｉｃａｔｉｏｎ　Ｎｕｍｂｅｒ　ＷＯ　９３／１２５４２）にも示されているようなものがある。その基本構造は、図７に示すように絶縁性基板３上に強誘電体薄膜２を上部電極５と、下部電極６とを挟んで積層した構造であった。
【０００４】
【発明が解決しようとする課題】ビスマス層状強誘電体は残留分極に結晶軸に対する異方性があり、最大残留分極が得られるのはａ軸方向で、ｃ軸方向の残留分極は非常に小さいことがわかっている。ところがこの材料を薄膜化する場合、スパッタ法や蒸着法等の物理的気相成長（ＰＶＤ）法や化学的気相成長（ＣＶＤ）法等の従来の成長方法ではｃ軸配向膜が得られやすく、最大の分極軸方向を基板面に垂直な方向に配向させることが難しかった。このため基板面と垂直方向に電界を印加する構造である従来の素子構造では有効に残留分極を利用できず、素子の微細化、低電圧化が難しいという問題があった。
【０００５】また一般的にビスマス層状強誘電体薄膜成膜時には７００Ｃ以上の高温が必要でなおかつ酸化雰囲気中にさらされるため、下部電極、強誘電体、上部電極の積層構造では強誘電体成膜時には下部電極と強誘電体の反応、下部電極の酸化による導通不良がおこり、良好な特性の素子を作製することが困難であった。
【０００６】本発明の目的は、上記従来の欠点を解消したキャパシタの構造及び製造方法を提供することにある。
【０００７】
【課題を解決するための手段】本発明は、絶縁性基板上にｃ軸配向ビスマス系層状強誘電体及び電極を有するキャパシタにおいて、前記強誘電体中の少なくとも一部分に基板面と平行な方向の電界を発生する第１、第２の電極からなる一対の電極が、前記強誘電体に接して設けられていることを特徴としている。このとき、電極は、ｃ軸配向ビスマス系層状強誘電体の最大分極方向に最大の電界が印加される位置に設けられていることによりいっそうの低電圧化がはかれるために好ましい。
【０００８】また本発明によるビスマス系層状強誘電体キャパシタの製造方法は、基板上にｃ軸配向ビスマス系層状強誘電体を形成し、パターニングする第１の工程と、前記強誘電体に１対の電極を形成する第２の工程とからなることを特徴としている。ここで、強誘電体を形成した後、もしくはパターニングを行った後に前記強誘電体の最大分極方向を検出すれば、検出された最大分極方向に電界を印加しうる１対の電極をパターニングされた強誘電体表面に形成することもできる。
【０００９】
【作用】図１に本発明によるキャパシタ構造を示す。一対の電極を用いて、絶縁性基板上のｃ軸配向ビスマス層状強誘電体に基板面と平行な電界を印加することにより、基板面に平行な面内に制限されているａ軸方向の残留分極を有効に利用することができる。即ち小さい電極面積で必要な電荷を得られるため素子の微細化を図ることができる。また電極を強誘電体成膜後に作製することにより、高温下での、強誘電体膜と電極との反応や、電極の酸化が抑制され、素子の信頼性の向上をはかることができる。さらに、最大分極軸方向が基板面に平行な面内で主に１方向にそろっている場合は、更に有効電荷密度が高くなるので、より小さい電界でキャパシタの分極反転が可能となりさらなる低電圧化が可能である。
【００１０】
【実施例】
（実施例１）ビスマス層状強誘電体としてストロンチウム酸タンタル酸ビスマス（$SrBi_2Ta_2O_9$、以下

ＳＢＴ）、絶縁性基板として表面酸化処理されたシリコン基板、電極材料としてWを用い、ＳＢＴの成膜方法としてＲＦマグネトロンスパッタを用いた場合の実施例を図２に示す。キャパシタ作製手順は次の通りであった。表面酸化処理されたシリコン基板上にＲＦマグネトロンスパッタ法で１μm 厚のＳＢＴを作製すると、基板温度７００Ｃ以上でｃ軸に配向したＳＢＴ薄膜が形成された。続いてこのＳＢＴ薄膜を底面０．５μm ×５μm 、高さ１μm の凸構造にエッチング加工した後、ＣＶＤ法でWを０．３μm の厚さに堆積した。その後ＳＢＴ凸構造の１μm ×５μm の側面、それからつながる引き出し電極を残してWをエッチング除去した。このとき１μm ×５μm の面の２つの引き出し電極は、他の素子の同一側面からの引き出し電極とつながっており、複数のキャパシタを並列に接続した構造となっている。この構造のキャパシタで得られたヒステリシス特性を図３に示す。比較対象として上部と下部のＰｔ電極で強誘電体を挟んだ従来構造の特性も同時に示した。上下に電極が積層された場合（一点鎖線）は残留分極値が１．４μＣ／cm^2と非常に小さいのに対し、基板に平行な電界を印加した場合（実線）は１０．５μＣ／cm^2となり残留分極値の著しい増加が見られ、素子の高密度化が図れることが示された。

【００１１】（実施例２）ビスマス層状強誘電体としてストロンチウム酸ニオブ酸ビスマス（$SrBi_2Nb_2O_9$、以下ＳＢＮ）、またはチタン酸ビスマス（$Bi_4Ti_3O_{12}$、以下ＢＩＴ）、絶縁性基板として表面処理されたシリコン基板、電極材料としてWを用い、成膜方法としてＲＦマグネトロンスパッタを用いた場合を示す。キャパシタ作製手順は実施例１と同様である。この構造のキャパシタで得られた強誘電特性を表１に示す。残留分極の絶対値は小さいがＳＢＴ膜の場合と同様に基板に平行な電界を印加した場合は残留分極値の増加が見られ、素子の高密度化が図れることが示された。

【００１２】

【表１】

強誘電体	印加電界（ｋＶ／ｃｍ）	上下積層型の残留分極値（μＣ／cm^2）	本発明型の残留分極値（μＣ／cm^2）
ＳＢＮ	３００	１．１	５．２
ＢＩＴ	２００	１．９	５．５

【００１３】（実施例３）絶縁体基板としてＭｇＯ単結晶（１００）面を用いて実施例１と同様の方法でＳＢＴを成膜し、実施例１と同様なキャパシタ構造を形成した。この場合ＳＢＴ薄膜はＭｇＯ基板に対してエピタキシャル成長するため基板に平行な面内でも分極方向がそろっていた。電界を印加する方向を決定するため、ＳＢＴ膜表面上に図４の様なドット状の電極群を作製し、電極Ａと電極ＢからＦの間でそれぞれ２端子法により残留分極を測定した。測定結果の一例を図５に示す。この場合では電極Ａと電極Ｄの間での分極値がもっとも大きくこの方向が最大分極軸方向であることがわかった。この結果に従い、電極Ａ－Ｄ方向と平行に電圧が印加されるように電極を形成した。この構造のキャパシタで得られた分極のヒステリシス特性を図６に示す。比較対象としてＰｔ電極が上部と下部に形成された同一試料の特性を示す。上下に電極が積層された場合（一点鎖線）はほとんどヒステリシス特性を示さないのに対し、基板に平行な電界を印加した場合（実線）は１３．７μＣ／cm^2となり残留分極値の著しい増加が見られた。実施例１の基板に平行な電界を印加した場合に比べても残留分極値で３０%増加し、抗電界で２２%減少しており、素子の高密度化、低電圧化が図れることが示された。

【００１４】なお、以上の実施例で用いた材料は２、３の例であり、本発明は、以上の実施例で述べた材料に限定されず、ｃ軸配向強誘電体で、最大分極方向がｃ軸に一致しない全ての材料に適用することが可能である。

【００１５】

【発明の効果】本発明による素子構造を用いることによりビスマス層状強誘電体の残留分極の有効な利用が達成でき、結果的に素子の高密度化、駆動電圧の低減が可能である。さらに下部電極の導通不良が減少し高信頼化が実現できる。

【図面の簡単な説明】

【図１】本発明によるキャパシタ構造を示す図である。

【図２】作製したキャパシタ素子構造を示す図である。

【図３】作製したキャパシタ素子のヒステリシス特性を示す図である。

【図４】電界印加方向を決定するためのドット状電極群を示す図である。

【図５】ドット状電極間の残留分極値を示す図である。

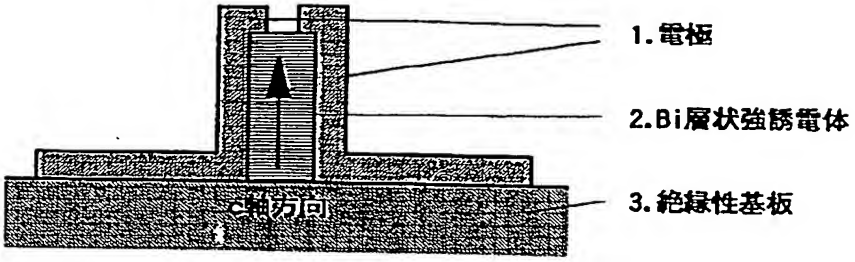
【図６】絶縁性基板として単結晶基板を用いた場合のキャパシタ素子のヒステリシス特性を示す図である。

【図７】従来法の薄膜キャパシタ構造を示す図である。

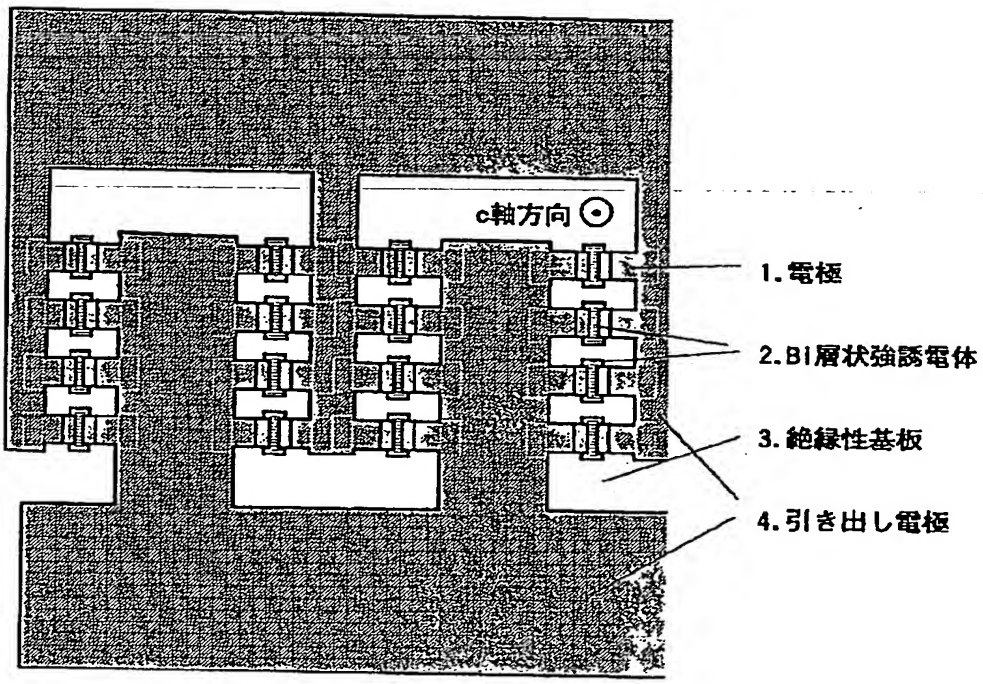
【符号の説明】

１　電極
２　ビスマス層状強誘電体
３　絶縁性基板
４　引き出し電極
５　上部電極
６　下部電極
７　ドット状電極

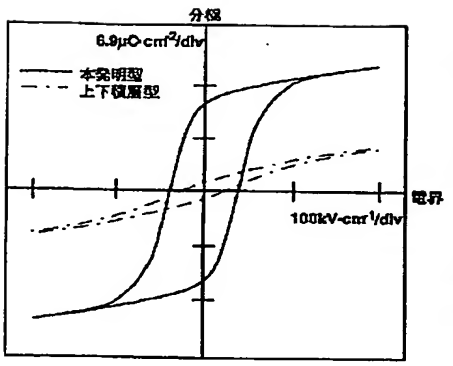
【図１】



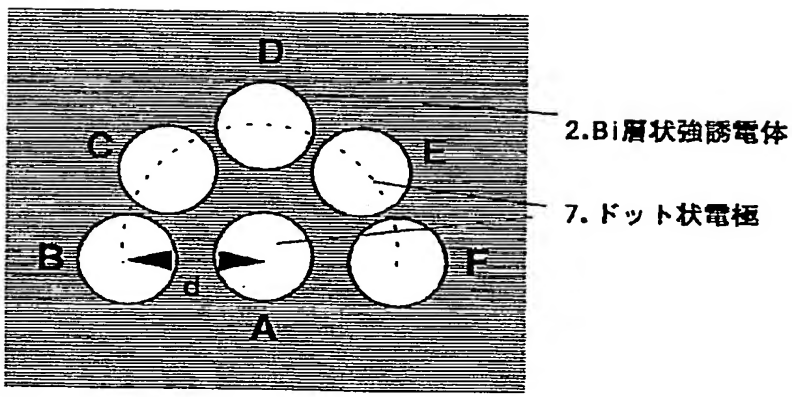
【図２】



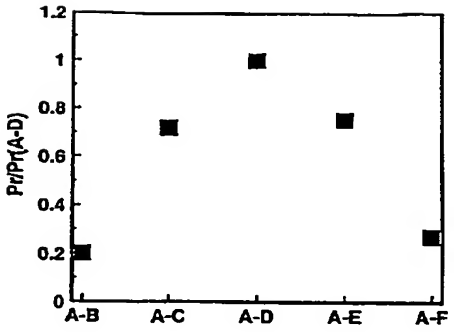
【図３】



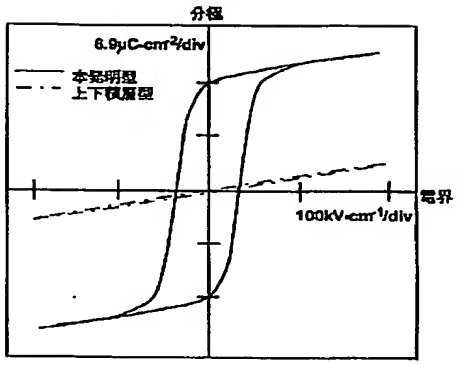
【図４】



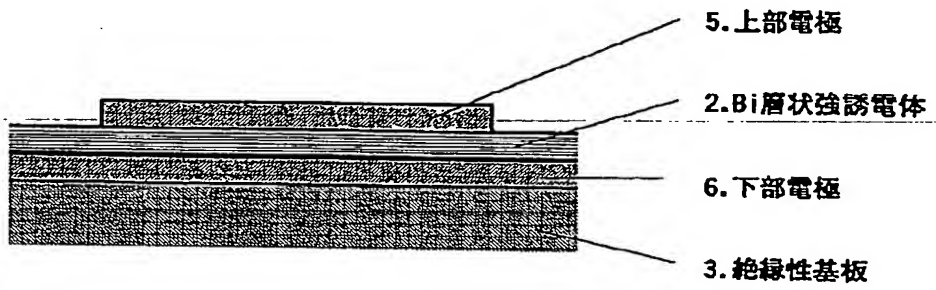
【図５】



【図６】



【図７】



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